APPARATUS FOR CONVERTING PCM SIGNAL

CLAIM OF PRIORITY

5   This application makes reference to, incorporates the same herein, and claims all

benefits accruing under 35 U.S.C. §119 accruing from an application entitled, *PCM*

CONVERTER, earlier filed in the Korean Industrial Property Office on July 11, 1998, and

there duly assigned Serial No. 1998-28061.

10   **BACKGROUND OF THE INVENTION**

1.   Field of the Invention

The present invention relates to an apparatus for converting pulse code modulation

(PCM) signal, and more particularly, the present invention relates to a PCM signal conversion

15   apparatus capable of providing compatibility between two different coding standards, namely,

A-law and μ-law in a communication system.

2. Description of the Related Art

A device typically found in digital communication systems is a converter for

20   converting an analog signal to a digital signal. Typically, PCM technique is implemented for

converting an analog signal to a digital signal. The PCM signal contains a plurality of groups

of multi-bit digital signals constituting a series of multi channel signals. The PCM technique

can be classified into two types of coding; A-law PCM coding (simply called A-law coding

herein after), which is widely used in Europe, and μ-law PCM coding (simply called μ-law

coding hereinafter), which is widely used in US and Japan.

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Currently, the A-law coding and the μ-law coding are both widely used in many

countries, as a result, there is a demand for a separate device for interfacing between the A-law

coding and the μ-law coding.

10   FIG. 1 illustrates a conventional code conversion circuit of the type having a ROM

(read only memory) for receiving at its address input, a digital trunk card including a time

switch/digital signal processor (DSP) (called a time switch/DSP hereinafter), a main control

card including a main time switch, and a digital trunk, the circuit used for converting the

signals encoded by different coding standards.

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Referring to FIG. 1, the system employs the μ-law coding, wherein signals B and D

represent A-law modulated (or encoded) signals and signals A and C represent μ-law

modulated signals. A digital signal from an office line is supplied to the main time switch 112,

passing through a digital trunk 124 and a time switch/DSP 122. The time switch/DSP 122

20   converts the A-law modulated signal B into the μ-law modulated signal A.   The time

switch/DSP 122 first receives the A-law modulated code value B and outputs a stored μ-law

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modulated value corresponding to the received A-law modulated signal B as linear code value, and then replaces the linear code value with corresponding μ-law modulated value from an pre-determined internal memory table. Accordingly, the A-law modulated signal B is converted into the μ-law modulated signal A and subsequently transmitted to a main control card 110.

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In contrast, when a signal is output to the office line from the system, the μ-law modulated signal C output from the main control card 110 is applied to the time switch/DSP 122. The time switch/DSP 122 then converts the μ-law modulated signal C into corresponding A-law modulated signal D from the pre-determined internal memory table using the above

10 process in reverse order. As a result, the converted A-law modulated signal D is supplied to the office line via the digital trunk 124.

All the signals, A, B, C and D, as shown in the Fig. 1, are digital signals (or PCM signals). The signals A and C represent the μ-law modulated signals while the signals B and

15 D represent the A-law modulated signals. As shown, the above known converter indiscriminately converts every channel signal in the multi-channel signals. However, it has the some disadvantages in operating that way. First, the design of the above conversion apparatus is complicated, which results in a high fabrication cost and complicates the overall size of the system. Moreover, since all the channel signals of the multi-channel signals are

20 converted indiscriminately, it is not suitable for selectively converting only one or two channel signals of the multi channel signals.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an economical conversion

5   apparatus capable of providing compatibility between two different coding standards with

respect to only selected channels.

To achieve the above object, there is provided an apparatus for converting PCM signals

in a system between two different modulation standards, namely A-law and μ-law. Such

10   apparatus includes a channel selector for generating a channel select signal to designate at least

one channel signal in multi-channel system. A plurality of input digital signals are received

in different channel signals. The apparatus further comprising a first codec for demodulating

the input digital signal, modulated by the first modulation standard in response to the channel

select signal, into an analog signal which is to be supplied to a second codec, and for

15   modulating an analog signal input from the second codec into digital signal to be modulated

by the first modulation standard; the second codec for demodulating the signal, modulated by

a second modulation standard in response to the channel select signal, into an analog signal

which is to be supplied to the first codec and for modulating the analog signal input from the

first codec into digital dignal to be modulated by the second modulation standard.

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A first mixer haivng a first buffer and a second buffer for selectively operating in response to a first mixing control signal generated from the channel selector, and a second mixer having a third buffer and a fourth buffer for selectively operating in response to a second mixing control signal generated from the channel selector, wherein the first buffer for receiving

5   the first input digital signal from the second codec responsive to channel select signal, a second buffer sharing an output terminal of the first buffer for receiving the digital signal supplied to the first codec wherein the first and second buffers operate complementarily to each other, a third buffer for receiving the digital signal output from the first codec responsive to the channel select signal, and a fourth buffer sharing an output terminal with the third buffer for receiving

10   a second input digital signal supplied to the second codec and the third and fourth buffers operate complementarily to each other.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a common PCM system;

5   FIG. 2 is a diagram illustrating a structure of a conversion apparatus according to an embodiment of the present invention;

FIG. 3 is a detailed diagram illustrating a structure of a codec (210) of the FIG. 2 according to an embodiment of the present invention; and,

10   FIG. 4 is a diagram illustrating waveforms of the respective signals used in the conversion apparatus according to the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described hereinbelow with referent to the accompanying drawings. There are a 32-channel PCM signal and a 24-channel

5   PCM signal, and the present invention incorporates the 32-channel PCM signal as an illustrative example, and all PCM signals would be referred to as a digital signal. Furthermore, the description of various features and structures of the present invention that are known to one skilled in the art are omitted for the sake of clarity and brevity. The present invention provides a codec apparatus as shown in FIG 2, which replaces the time switch/DSP 122 of the Fig. 1,

10   for converting a digital signal to the converted analog signal and an analog signal to a digital signal.

Referring to FIG. 2, the codec apparatus includes a codec 210, a channel selector 212 for generating a channel select signal, S_FS and a first mixer 214 and a second mixer 216. The

15   channel selector 212 outputs the channel select signal S_FS and mixing control signals J and K, which are controlled by a clock signal CLKx, a frame sync signal FSx, an read address, and data input. One skilled in art would know that that are various ways and type of circuits served to provide an address generator controlled by a clock signal from a clock domain, which can generate read address for reading out data from the data storage elements. The codec 210 has

20   input/output terminals for receiving and supplying the A-law modulated digital signals B and D, respectively, and input/output terminals for receiving and supplying the μ-law modulated

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digital signals A and C, respectively. The codec 210 selectively converts a specified channel

signal from the modulated multi channel signals in response to the channel select signal, S_FS

generated by the channel selector 212. The first mixer 214 includes two buffers operating

complementarily to each other in response to the mixing control signal J, a first buffer 214a for

5   storing the digital signal output E from the codec 210 and a second buffer 214b for storing the

original digital signal B. Similarly, the second mixer 216 consists of two buffers operating

complementarily to each other in response to the mixing control signal K, a third buffer 216a

for storing the digital signal output H from the codec 210 and a fourth buffer 216b for storing

the original digital signal C. Each pair of the buffers in each mixer share the output terminal

10   and operate complementarily to each other in such a manner that first buffer is enabled while

the second buffer is disabled, and vice versa.

Referring to FIG. 3, the codec 210 consist of an A-law codec 320 and a μ-law codec

310, the digital signals S and Q represent A-law modulated signals and digital signals P and

15   R represent μ-law modulated signals. The present invention incorporates extensively used

commercial codec, as an example illustration, since these are inexpensive and easily available.

However, those skilled in art would know that other equivalent commercial codec can be

incorporated to make the present invention to work to achieve the same objects and goals of

the present invention. Accordingly, the preferred embodiment incorporates a commercial codec

20   TP3057 for A-law codec. The A-law codec 320 demodulates the A-law modulated digital

signal S into an analog signal to be supplied to the μ-law codec 310, and also modulates an

analog signal output received from the μ-law codec 310 into the A-law modulated digital signal

Q. The present invention incorporates a commercial codec TP3054 as the μ-law codec 310.

The μ-law codec 310 demodulates the μ-law modulated digital signal R into analog signal to

be supplied to the A-law codec 320. Also, it modulates the analog signal output from the A-law

5   codec 320 into the μ-law modulated digital signal P. The μ-law codec 310 and A-law codec

320 determine which channel signals of the multi channels to be modulated or demodulated

in response to the frame sync signal FSx, clock signal CLKx, and the channel select signal

S_SF from the signal channel selector 212.

10   FIG. 4 illustrates waveforms of the respective signals used in the codec apparatus

according to the present invention as follow: the frame sync signal (FSx), the clock signal

(CLKx), the channel select signal (S_FS), and a 8 bit signal ranging from 0 bit to 7 bit (D0-D7)

constituting one channel. As shown in FIG. 4, one channel has time duration of 3.9μsec and

accordingly, the channel select signal also has time duration of 3.9μsec. The channel selector

15   212 generates the channel select signal (S_FS) using the frame sync signal (FSx), the clock

(CLKx), the address input via an address bus and the data input via a data bus.

In the specification, the description will be given on the assumption that the signals B

and D are A-law modulated digital signals, and the signals A and C are μ-law modulated digital

20   signals. In such condition, the signals A and C represent μ-law modulated (or encoded) signals

and the signals B and D represent A-law modulated signals, the signals F, H, E and G of FIG.

2 correspond to the signals S, Q, P and R of FIG. 3, respectively. However, It will be

understood by those skilled in this art that the invention can be applied to such different

embodiments where the signals B and D are μ-law modulated digital signals and the signals

A and C are A-law modulated digital signals. In the later embodiment, the signals A and C are

5   considered to be the A-law modulated signals and the signals B and D are μ-law modulated

signals, the signals F, H, E and G of FIG. 2 would correspond to the signals R, P, Q and S of

FIG. 3, respectively.

Now, a description will be given as to an operation of converting the A-law modulated

10   signal B or F into the μ-law modulated signal E as shown in Fig.2. The signal B is applied to

a mixer 214 and the signal F identical to the signal B is applied to the codec 210. The codec

210 selects one channel to be converted from the signal F having multiple channels (e.g., 32

channels) in response to the channel select signal S_FS generated from the channel selector

212. The channel select signal S_FS is synchronized with the incoming channel signals

15   constituting signal F. After selecting a specific channel in response to the channel select signal

S_FS, the codec 210 converts the selected channel of the A-law modulated signal F (or B) into

the μ-law modulated signal.

The above steps can be understood easily by the illustration shown in FIG 3. Upon a

20   reception of the signal S identical to the signal F, the A-law codec 320 demodulates one

channel of the A-law modulated signal F selected by the channel select signal S_SF into an

analog signal. The demodulated analog signal is then applied to the μ-law codec 310 which in turn modulates the analog signal to generate the μ-law modulated digital signal P which is identical to the signal E of FIG. 2.

5   Referring to FIG. 4, the channel select signal S_FS, for selecting a specific channel, is synchronized with the period of one corresponding channel, and maintains a high state for 3.9μsec. The channel select signal S_FS selects specific first frame, CH#0, in response to the frame sync signal FSx and one specific channel which contains the 8 bit signal ranging from 0 bit to 7 bit (D0-D7).

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          In the meantime, the channel select signal S_FS is supplied to the first mixer 214 as a mixing control signal J. For the duration of the signal J (i.e., 3.9μsec), the first mixer 214 blocks an output path of the second buffer 214b of the first mixer 214 from transmitting the buffered B signal, and connects an output path of the first buffer 214a of the first mixer 214 for

15   the transmission of the signal E. Thus, for the duration of the channel select signal S_FS (3.9μsec), the first mixer 214 selectively outputs the signal E while cutting off the signal B received thereon. Accordingly, if the signal B comprises 32 channels, only one channel selected in response to the channel select signal S_FX, is modulated by μ-law coding, and the remaining 31 unselected channels are output to the first mixer 214 without any conversion

20   operated thereon by the codec 210.

Referring to FIG2, a brief description will be given as to an operation of converting the μ-law modulated signal C (or G) into the A-law modulated signal H. Initially, the signal C is applied to the second buffer 216b of the second mixer 216, and the signal G (or C) is applied to the codec 210. The of the codec 210 selects a specific channel to be converted from the

5   signal C, which comprises multiple channels (e.g., 32 channels), in response to the channel select signal S_FS generated from the channel selector 212. Then, the codec 210 converts the selected channel on the μ-law modulated signal G(or C) on the selected channel into the A-law modulated signal H.

10   More detailed functions of the codec 210 is further described by following the features shown in FIG 3. Upon reception of the signal R identical to the signal G, the μ-law codec 310 demodulates the selected channel of the μ-law modulated signal R (or G) in response to the channel select signal S_SF into an analog signal. The demodulated analog signal is supplied to the A-law codec 320, in turn the A-law modulates the analog signal into the A-law modulated signal Q, which is identical to the signal H of FIG. 2.

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In the meantime, the channel select signal S_FS is supplied to the second mixer 216 as a mixing control signal K. For the duration of the signal K (i.e., 3.9μsec), the second mixer 216 blocks an output path of the second buffer 216b of the second mixer 216 from transmitting the

20   stored signal C, but connects an output path of the first buffer 216a of the second mixer 216 for the transmission of the signal H. Thus, for the duration of the channel select signal S_FS

(3.9μsec), the second mixer 216 selectively outputs the signal H while cutting off the signal C. Accordingly, if the signal C has 32 channels, only one channel selected by the channel select signal is modulated by A-law coding and the remaining 31 unselected channels are output without any conversion operated thereon by the codec 210.

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The present invention can convert one channel selected channels out of the A-law modulated channel signals into the μ-law modulated signal, and vice versa. That is, it provides compatibility between two different modulation standards. Although the invention has been described with reference to selectively modulating only one channel signal, it is also possible

10 to selectively modulate maximum of four channel signals with the channel selector 212 of FIG. 2. In such case, the number of codec 210 and the mixers 214 and 216 should be increased as many as the number of the channels to be converted.

As described above, the present invention provides an apparatus for converting PCM

15 signals which can selectively convert a number of selected channels from the multi channel signals using known commercial codec, and further helps to reduce the fabrication cost and the overall size of the system.

While the invention has been shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in

20 form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.